St. Philomena's College Autonomous, Mysore

PG Department OF COMPUTER SCIENCE

Question Bank (Revised Curriculum 2020 onwards)

First Year- First Semester (2020 -22 Batch)

Course Title (Paper Title): COMPUTER ORGANIZATION AND ARCHITECTURE(HC)

QP CODE:86123

Unit	Sl.no	Question	Marks
1	1.	Define micro computer	2
1	2.	What is laptop computer?	2
1	3.	Define work station	2
1	4.	What is super computer?	2
1	5.	Define main frame computer.	2
1	6.	What is hand held computer?	2
1	7.	What are PC and IR in Basic organizational concept?	2
1	8.	Define MAR and MDR.	2
1	9.	Define Bus	2
1	10.	What is programming software?	2
1	11.	Define application software.	2
1	12.	What is multiprocessor computer?	2
1	13.	Define error and list error detection mechanisms	2
1	14.	What are even parity and odd parity?	2
1	15.	Define system software.	2
2	16.	Define instruction	2
2	17.	What is instruction bit	2
2	18.	What are DR and AR in registers	2
2	19.	What are AC and TR in registers	2
2	20.	Define INPR and OUTR	2
2	21.	Write instruction register format for register reference	2
2	22.	Write instruction register format for memory reference	2
2	23.	Write instruction register format for input or output reference	2
2	24.	Draw flowchart for instruction cycle	2
2	25.	List out different addressing modes	2
2	26.	What is data movement and arithmetic type instruction	2
2	27.	What are bit manipulation and I/O type of instruction	2
2	28.	What are Boolean and special purpose type of instruction	2
2	29.	Define hardwired control unit	2
2	30.	What is micro programmed control unit	2
3	31.	Define micro operations.	2
3	32.	Define a register	2
3	33.	What are arithmetic micro operations?	2
3	34.	List out the arithmetic micro operations.	2
3	35.	What is binary adder?	2

3	36.	Define logical micro operations.	2
3	37.	List out the logical micro operations	2
3	38.	List all the shift micro operations.	2
4	39.	Write memory hierarchy diagram.	2
4	40.	Define memory.	2
4	41.	Define cache memory.	2
4	42.	What is virtual memory	2
4	43.	Mentions the differences between isolated IO interface and memory mapped IO interface	2
4	44.	Define cache coherence problem	2
4	45.	List out the different interconnection structures methods	2
1	46.	Explain performance evaluation of a program	5
1	47.	Explain bus structure.	5
1	48.	Illustrate the following using hamming code 1011	5
1	49.	Illustrate the following using Booth's algorithm 5 and 3	5
1	50.	Illustrate the following using division algorithm 13 and 4	5
1	51.	Illustrate the following using cyclic redundancy check X^3+1 and 10111011	5
1	52.	Illustrate the following using hamming code 1001	5
1	53.	Illustrate the following using Booth's algorithm 7 and 2	5
1	54.	Illustrate the following using division algorithm 11 and 3	5
1	55.	Illustrate the following using cyclic redundancy check X^3+x^2+1 and10110110	5
1	56.	Draw flowchart for division algorithm.	5
1	57.	Draw flowchart for booth's algorithm.	5
2	58.	Explain instruction cycle	5
2	59.	What is stack organization?	5
2	60.	Define register stack?	5
2	61.	What is memory stack?	5

2	62.	Explain immediate addressing mode?	5
2	63.	Explain implies addressing mode?	5
2	64.	Explain direct addressing mode?	5
2	65.	Explain indirect addressing mode?	5
2	66.	Explain register indirect addressing mode?	5
2	67.	Explain register addressing mode?	5
2	68.	Explain relative addressing mode?	5
2	69.	Explain indexed addressing mode?	5
2	70.	Explain base register addressing mode?	5
2	71.	Explain auto increment addressing mode?	5
2	72.	Explain auto decrement addressing mode?	5
2	73.	Explain three instruction format?	5
2	74.	Explain two instruction format?	5
2	75.	Explain one instruction format?	5
2	76.	Explain zero instruction format?	5
2	77.	List out the differences between hardwired control and micro programmed control	5
2	78.	Mention the properties and characteristics of CISC architecture	5
2	79.	Illustrate the advantages and dis advantages of CISC architecture	5
2	80.	Mention the properties and characteristics of RISC architecture	5
2	81.	Illustrate the advantages and disadvantages of RISC architecture	5
2	82.	Differentiate RISC and CISC architecture	5
3	83.	Explain register transfer language.	5
3	84.	Explain bus and memory transfer.	5
3	85.	Illustrate binary adder	5
3	86.	Illustrate adder-subtractor	5
3	87.	Explain binary incrementer	5
3	88.	Explain logical shift operation in shift micro operations	5
3	89.	Explain circular shift operation in shift micro operations	5
3	90.	Explain arithmetic shift operation in shift micro operations	5
4	91.	Mention the advantages and disadvantage of cache memory	5
4	92.	Mention the characteristics of primary memory	5
4	93.	Mention the characteristics of secondary memory	5
4	94.	Explain SRAM	5
4	95.	Explain DRAM	5
4	96.	Explain the registers used in DMA	5
4	97.	What are the characteristics of multiprocessor	5
4	98.	Explain static arbitration in inter processor arbitration	5
4	99.	Explain dynamic arbitration in inter processor arbitration	5
4	100	Explain time shared common bus method in interconnection structure	5
4	101	Explain multiport method in interconnection structure	5
4	102	Explain crossbar switching method in interconnection structure	5
4	103	Explain multistage switching method in interconnection structure	5

4	104	Explain hypercube system method in interconnection structure	5
4	105	Explain daisy chaining in interrupt initiated IO data transfer	5
4	106	Explain parallel priority encoder in interrupt initiated IO data transfer	5
1	107	Explain different types of computers based on their performance and capacity.	10
1	108	Explain functional units of computer.	10
1	109	Explain basic operational concepts.	10
1	110	Explain hamming code error detection correction mechanism with example.	10
1	111	Draw flowchart for addition and subtraction algorithm.	10
1	112	Perform 1's complement arithmetic operation for the following a. -2+5 b. +3-8 c. -4-9 d. +7-12 e. +6-13	10
1	113	Perform 2's complement arithmetic operation for the following a. +2-3 b. +4-1 c. -5-7 d. -3-9 e. 12-4	10
1	114	Explain cyclic redundancy check error detection mechanism with example	10
2	115	Explain register stack and memory stack	10
2	116	Explain register addressing and register indirect addressing mode?	10
2	117	Explain direct addressing mode and indirect addressing mode?	10
2	118	Explain relative addressing mode and indexed addressing mode?	10
2	119	Explain auto increment addressing mode and auto decrement addressing mode?	10
2	120	Explain implied addressing mode and base register addressing mode?	10
2	121	Explain three instruction format and two instruction format?	10
2	122	Explain one instruction format and zero instruction format?	10
2	123	Explain references in computer instructions.	10
2	124	Illustrate different types of instructions.	10
2	125	Explain RISC architecture.	10
2	126	Explain CISC architecture	10
3	127	What are the applications of logical micro operations	10
3	128	Explain logical shift and circular shift operation in shift micro operations	10
3	129	Explain logical shift and arithmetic shift operation in shift micro operations	10
3	130	Explain arithmetic shift and circular shift operation in shift micro operations	10
3	131	What are control memory?.explain	10
3	132	Explain arithmetic logic shift unit	10
3	133	Explain address sequencing	10
3	134	Explain design of control unit in micro programmed control unit	10
4	135	Write a note on RAM	10

4	136	Write a note on ROM	10
4	137	Illustrate virtual memory	10
4	138	Explain IO interface	10
4	139	Explain programmed mode of data transfer	10
4	140	Write a note on interrupt initiated IO data transfer	10
4	141	Explain Direct Memory Access (DMA)	10
4	142	write a note on inter process arbitration	10

Question Paper Pattern- Blue Print

Department: PG Computer Science			
Subject Name: Computer Organization and Architecture			
Duration: 03 Hrs			**Total marks=70**
PART A			
1	**Answer any FIVE of the following**		**5x2=10**
a	Unit 1		
b	Unit 1		
c	Unit 2		
d	Unit 3		
e	Unit 4		
f	Unit 4		
g	Unit 4		
PART B			
Answer any ONE FULL question from the following			**4x15=60**
2	a	Unit 1	15
	b	Unit 1	
OR			
3	a	Unit 1	15
	b	Unit 1	
4	a	Unit 2	15
	b	Unit 2	
OR			
5	a	Unit 2	15
	b	Unit 2	
6	a	Unit 3	15
	b	Unit 3	
OR			
7	a	Unit 3	15
	b	Unit 3	

8	a	Unit 4	15
	b	Unit 4	
OR			
9	a	Unit 4	15
	b	Unit 4	

MODEL QUESTION PAPER

Department: PG Computer Science				
Subject Name: Computer Organization and Architecture				
Duration: 03 Hrs				**Total marks=70**
PART A				
1	**Answer any FIVE of the following**			**5x2=10**
A	Define micro computer			
B	What is laptop computer?			
C	Define work station			
D	What are DR and AR in registers			
E	What are AC and TR in registers			
F	List all the shift micro operations.			
G	Write memory hierarchy diagram.			
PART B				
Answer any ONE FULL question from the following				**4x15=60**
2	a	Illustrate the following using division algorithm 11 and 3	5	15
	b	Illustrate the following using cyclic redundancy check X^3+x^2+1 and10110110	5	
	c	Draw flowchart for division algorithm.	5	
OR				
3	a	Explain instruction cycle	5	15
	b	Explain different types of computers based on their performance and capacity.	10	
4	a	Explain one instruction format?	5	
	b	Explain register stack and memory stack	10	
OR				
5	a	Explain relative addressing mode?	5	15
	b	Explain indexed addressing mode?	5	
	c	Explain base register addressing mode?	5	
6	a	Illustrate adder- subtractor	5	15
	b	Explain binary incrementer	5	

	c	Explain logical shift operation in shift micro operations	5	
OR				
7	a	Explain bus and memory transfer.	5	15
	b	Explain arithmetic logic shift unit	10	
8	a	Explain SRAM	5	15
	b	Write a note on RAM	10	
OR				
9	a	Explain the registers used in DMA	5	15
	b	What are the characteristics of multiprocessor	5	
	c	Explain static arbitration in inter processor arbitration	5	

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